An amplifier with AGC for the 80 Mbit/s Optical Receiver of the CMS digital optical link

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Abstract

An 80 Mbit/s amplifier has been developed for the optical receiver of the CMS tracker control link. Four channels of the circuit have been integrated in a 0.25 µm commercial CMOS process using radiation tolerant layout practices to achieve the required radiation tolerance. An Automatic Gain Control (AGC) loop allows for detection of wide dynamic range input signals (10 µA to 500 µA photocurrent) with minimum noise, compatible with the maximum expected radiation-induced drop in quantum efficiency of the PIN photodiode. A second feedback loop compensate a photodiode leakage current up to 100 µA.

1. INTRODUCTION

The CMS tracker control system will use approximately 1000 digital optical links for the transmission of timing, trigger and control signals [1]. These digital signals, transmitted serially at a bitrate of 40 Mbit/s (80 Mbit/s for the clock signal), will be converted into electrical signals by a PIN photodiode at the receiver end. As one of the transmission channel ends will sit inside the CMS detector, hence in a radiation environment, its components need to be radiation hard.

The front-end element of the optical receiver is a transimpedance amplifier, which has to amplify the photocurrent delivered by the PIN diode and detect the presence of a reset signal, coded in the foreseen protocol as missing pulses for more than 2 µs. In the CMS control system, the PIN diode is a commercial component and its performance will be affected by radiation. To compensate for the radiation-induced degradation of the photodiode quantum efficiency, the amplifier should have a wide dynamic range (current signals between 10 and 500 µA). Moreover, it should be able to compensate a photodiode leakage currents of up to 100 µA.

The amplifier circuit has to be radiation tolerant up to a total integrated dose of 10 Mrad. As no commercial amplifier satisfying all these conditions exists, the development of an ASIC was necessary. To meet all the specifications, a commercial 0.25 µm CMOS technology has been chosen for the development of the amplifier. This advanced technology allows to easily meet the speed requirements with minimum power consumption: the bandwidth of 80 MHz can be achieved without large currents, resulting in a power consumption below 25 mW per channel at the nominal voltage of 2.5 V.

Moreover, the thin gate oxide of this deep submicron process is inherently total dose hard, and the systematic use of enclosed (edgeless) NMOS transistors and guardrings allows the design of circuits with radiation tolerance exceeding the specified 10 Mrad [2]. Such design techniques have also been demonstrated to significantly increase the Single Event Latchup (SEL) immunity of the circuit [3].

2. CIRCUIT DESCRIPTION

The global architecture of the amplifier circuit is shown in Figure 1, and it is mainly composed of four blocks: a transresistance preamplifier, a chain of limiting gain amplifiers, an LVDS driver and a block to detect and generate the reset signal.

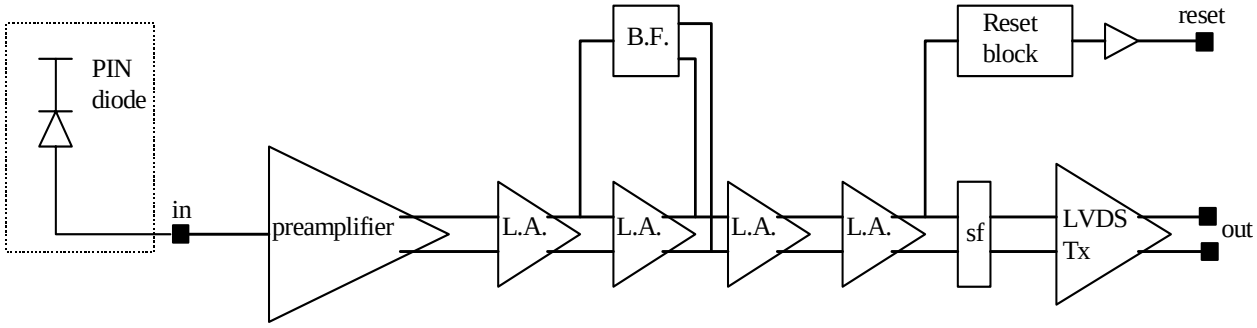

Figure 1: Global architecture of the amplifier circuit, DC connected to the external PIN diode. The transresistance preamplifier is followed by a chain of limiting amplifiers (L.A.), where a Balancing Feedback (B.F.) block ensures that the average of the two differential signals is identical.

The PIN diode is DC coupled to the preamplifier, which also supplies the bias voltage to the photodiode (about 1.8 V). This solution also allows for an easy integration of a feedback loop to sink the radiation-induced leakage current of the photodiode.

2.1 The preamplifier

The architecture of the preamplifier is shown in Figure 2. The transresistance amplifier transforms the current signal from the PIN diode into a voltage signal, with a variable transresistance. This sort of Automatic Gain Control (AGC) is necessary to cope with the large dynamic range required for the amplifier, from 10 to 500 µA current signals. The high gain on small signals, desired for high signal over noise ratios, is in fact incompatible with the big signals because the voltage excursion at the preamplifier output is limited. The presence of an AGC mechanism, other than ensuring a constant output signal irrespective of the input current, allows for optimum noise performance: maximum gain (maximum transresistance), hence minimum noise, is used for small signals.

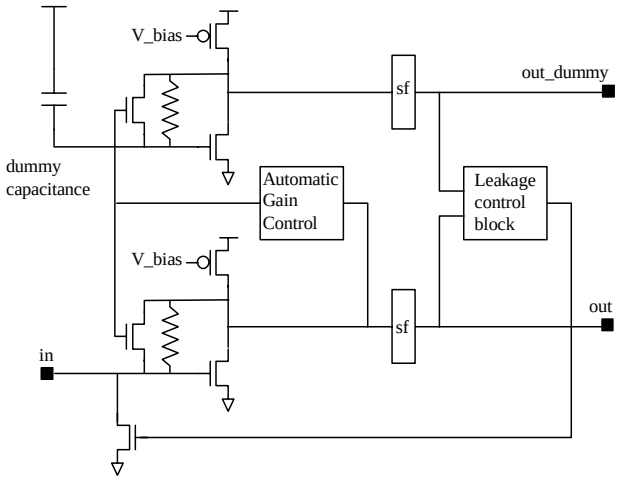

Figure 2: Architecture of the transresistance preamplifier. The two blocks marked “sf” are simple source followers.

The AGC is implemented by a transistor in parallel with the 16 kΩ polysilicon resistance, having its gate voltage controlled by a slow feedback loop. The AGC loop is actually a minimum detector followed by a slow transconductance amplifier acting as an integrator. For high input currents, this block detects a minimum signal below a fixed reference voltage and decreases the transresistance by acting on the feedback transistor gate. This feedback loop needs to be slow so as to be negligible at the signal frequency, as it needs only to compensate for the radiation-induced drop in the quantum efficiency of the photodiode. Such drop occurs during the whole LHC life cycle (10 years). The simulated transfer function of the preamplifier is shown in Figure 3, for both high and low signal levels. The transresistance changes from about 16 kΩ for a 10 µA signal to about 175 Ω for a 500 µA signal. Correspondingly, the bandwidth passes from 105 to 858 MHz.

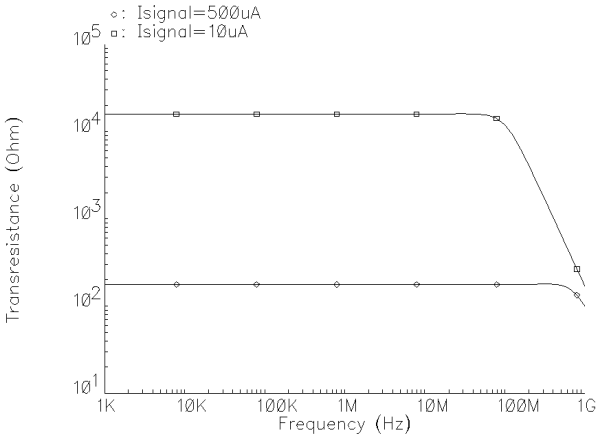

Figure 3: Transfer function of the preamplifier.

The single ended architecture chosen for the preamplifier front end allows the correct biasing of the PIN diode but, as all single ended structures, has an inherently poor Power Supply Rejection Ratio (PSRR) compared to differential architectures. To improve this important characteristic, a pseudo-differential scheme has been used. The transresistance input stage has been

replicated as a “dummy” circuit, as shown in the upper part of Figure 2. The output of both the true preamplifier and the dummy stage is used as the input to the differential limiting amplifier chain. Therefore, from the preamplifier output to the LVDS driver output, the signal is fully differential.

This pseudo-differential scheme requires good matching between the input capacitance of the true and dummy branches. To match the PIN diode capacitance, we have integrated a dummy capacitance at the input of the dummy branch. Its value has been chosen to match as well as possible the capacitance of the PIN diode after irradiation. In this way, the PSRR of the preamplifier will improve during operation, and finally be optimum when the signal delivered by the photodiode is at its minimum.

The output of the dummy circuit is moreover used as an input to the additional feedback loop controlling the photodiode leakage current sink. Two peak detectors, sampling the output signal from the true and dummy branches, and a slow transimpedance amplifier form the leakage control circuit, as shown in Figure 4. In the presence of a photodiode leakage current, the output maximum of the true branch tends to decrease. This decrease is detected by the leakage control circuit, which then acts on the gate of the sink NMOS transistor to drive the leakage current to ground and re-establish the equilibrium condition. As for the Automatic Gain Control, the leakage control feedback needs to be very slow compared with the lower signal frequency. In fact, this circuit has to compensate for the increase in the photodiode leakage current, which is a slow radiation-induced process occurring during the whole LHC life cycle.

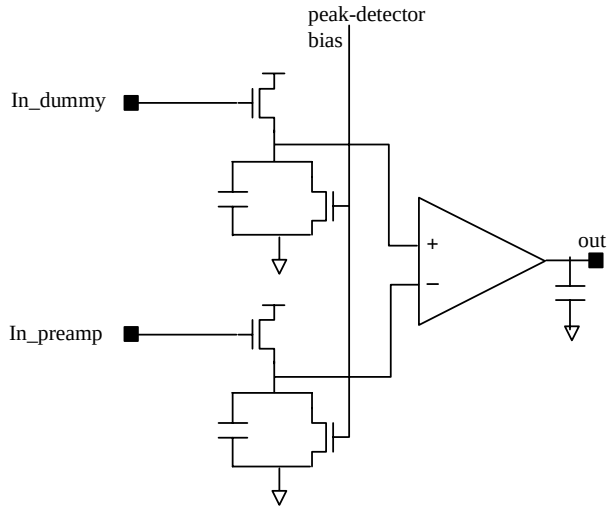

Figure 4: Architecture of the Leakage control block.

2.2 The limiting amplifier chain

The output of the preamplifier is not fully differential, the signal coming from the dummy branch being DC. The first limiting amplifier of the chain needs therefore to be unbalanced for its output signal to be fully differential. This is implemented through the action of a “balancing” feedback block, as shown in Figure 1. This circuit block senses the peak of the output signals from the second amplifier of the chain, and controls the current unbalance between the two output branches of the first amplifier. The amplifier chain performs an amplification of the signal and limits it to a pre-fixed peak-to-peak value, preparing it for optimum input to the LVDS driver.

The four amplifiers composing the chain are differential gain stages with diode-connected transistors as loads to limit the signal excursion. To linearize their output signal, a polysilicon resistance has been added between the two branches of each amplifier.

2.3 The LVDS driver

The specifications of the circuit require the output to be Low Voltage Differential Signaling (LVDS). LVDS is a high speed, low power general purpose interface standard using differential data transmission, and it is independent of a specific power supply [4]. The standard peak-to-peak signal is 400 mV, and the common mode voltage is 1.2 V. To generate the differential output voltage, a termination resistor (typically 100 Ω) is required at the receiver end.

The LVDS driver has been designed as a differential amplifier with load resistors. The use of resistors as loads achieves good signal linearity, and helps matching the impedance requirements of the driven transmission line. To correctly generate an LVDS signal, the value of the load resistors has been designed to be 275 Ω, with 4.7 mA current flowing in each branch. Such resistors have been integrated as high precision p-diffusion resistors (10% spread). The speed performance of the designed driver is well above the required 80 Mbit/s.

2.4 The reset block

The transmission protocol foresees that the reset signal is coded as missing pulses for a long time period (2 μs or more) [5]. The amplifier circuit is required to detect the transmission of the reset and respond to it by changing the status of a flag on a dedicated output line.

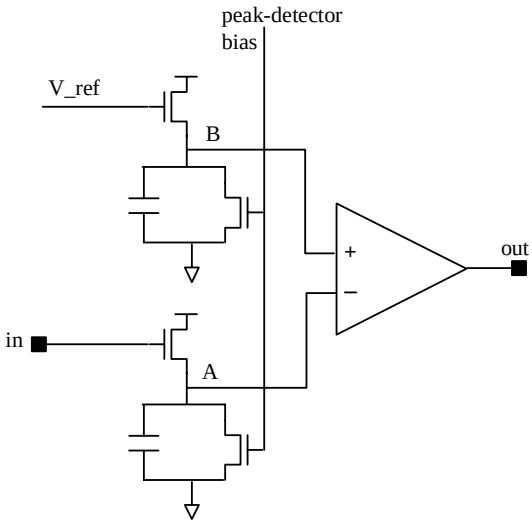

Figure 5: Architecture of the reset block.

To perform this task, we have integrated a reset block in the amplifier, connected to one of the differential outputs of the limiting gain amplifier chain as shown in Figure 1. The schematic of the reset block is depicted in Figure 5.

The input of the reset block is connected to a peak detector sensing the maximum of the signal. The output of the peak detector is compared with a reference voltage through a symmetrical operational amplifier. In the absence of a signal, the voltage at node A decreases with a time constant fixed by the value of the capacitance and of the current in the peak-detector circuit. If the absence of the signal is long enough, the voltage of node A eventually goes below the voltage of node B, and the output of the reset block changes.

3. CIRCUIT IMPLEMENTATION

3.1 Chip floorplan

The final ASIC includes 4 amplifier channels, each occupying an active area of 0.5x0.25 mm^2. A picture of the chip is shown in Figure 6. The vast majority of the chip area is unused, the die size of 2x2 mm^2 having been assigned to this circuit in the mainframe of a multi-project run. The distance amongst the pads has been chosen to be compatible with wire-bonding and low cost bump-bonding techniques. Input pads are on the left of the chip, LVDS output pads on the right, and the power is distributed along the y-axis with pads on both the top and bottom of the chip.

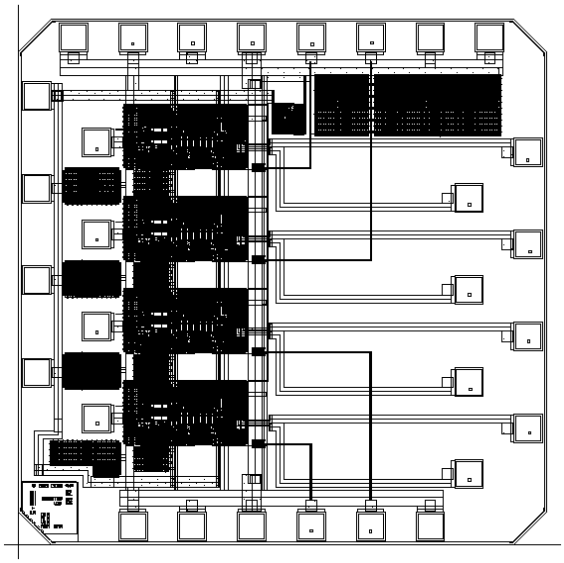
Figure 6: Layout view of the amplifier chip.

3.2 Radiation tolerance considerations

The total dose tolerance of the extremely thin gate oxide of transistors in the quarter micron technology used is well beyond the specified 10 Mrad level. Threshold shifts as low as 35 mV (for NMOS) and -70 mV (for PMOS) have been measured after an irradiation up to 30 Mrad [6]. Changes in mobility, transconductance and noise are also very limited after such a high total dose, always below 10%. Those radiation-induced changes are lower than the manufacturing spread in the same parameters. Therefore, the typical design procedure of varying the process parameters in the $\pm 3\sigma$ range should be sufficient to ensure the correct functionality of the circuit even after irradiation.

Special attention has been devoted to avoid possible leakage paths under the still thick lateral and field oxides. Enclosed layout geometry has systematically been used for NMOS transistors to prevent source-drain leakage currents. Moreover, all n+ diffusions at different potential have been isolated from each other by a p+ guardring completely surrounding it. Both techniques have been shown to be very effective [6,7], and the use of guardrings has the additional advantage of decreasing the Single Event Latchup (SEL) sensitivity of the circuit [8]. Robustness against Single Event Upset (SEU), which can generate errors in the transmitted data path, is embedded at the system level through the use of an adequate transmission code allowing error detection and correction (EDAC).

4. SUMMARY

We have developed an 80 Mbit/s amplifier for the optical receiver of the CMS tracker slow control optical link. The use of a commercial quarter micron CMOS

process enables us to meet the speed, low power and radiation hardness specifications for the amplifier. We used enclosed layout topology for all NMOS transistors, and guardrings to achieve the required level of total ionising dose tolerance.

The front-end of the circuit, a transimpedance preamplifier, has been designed to compensate for the radiation-induced performance degradation of the PIN photodiode: decrease in the signal amplitude and leakage current increase. AGC has been implemented to achieve optimum signal-over-noise ratio on both high and low level signals, corresponding to the maximum and minimum foreseen quantum efficiency of the photodiode. A feedback loop monitors the PIN diode leakage current and can compensate for its increase up to 100 μA.

Imbedded in the amplifier is a sub-circuit to detect the transmission of a reset signal. Upon detection, a flag is enabled on a dedicated output line.

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